

PICO Extreme™



PICO Extreme – the most advanced algorithmic synthesis enabling the most efficient hardware for complex algorithms

About the PICO Platform

The PICO platform comprises tools, IP based around an advanced compiler technology, and efficient hardware synthesis that finds and exploits parallelism at multiple levels. This allows designers to create efficient hardware from an untimed C algorithm. The PICO platform provides a comprehensive verification and validation environment, which includes SystemC TLM support and automatic RTL testbench creation. It also enables designers to build a library of reusable algorithmic IP for rapid use on a wide range of silicon technologies.

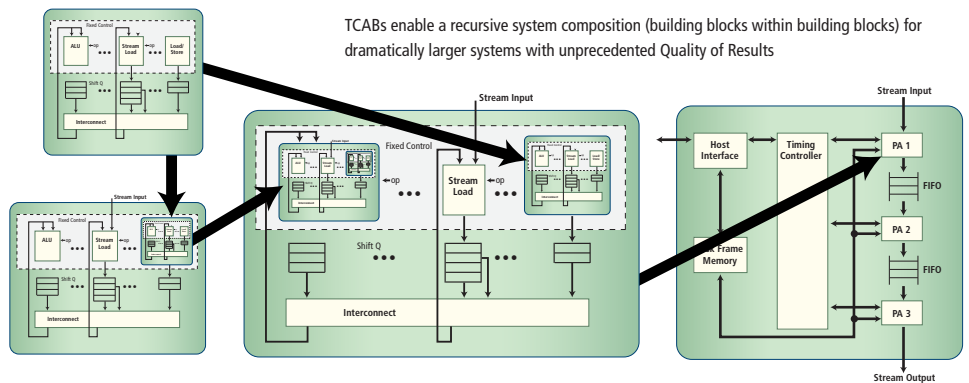
PICO Extreme

PICO Extreme represents a major advance in algorithmic synthesis. PICO Extreme introduces a major technology innovation (TCABs), an advanced clock gating scheme for reduced power consumption, data extraction and export for C-RTL equivalence checkers, and an OCP-IP compliant host interface.

Key Innovation: TCABs

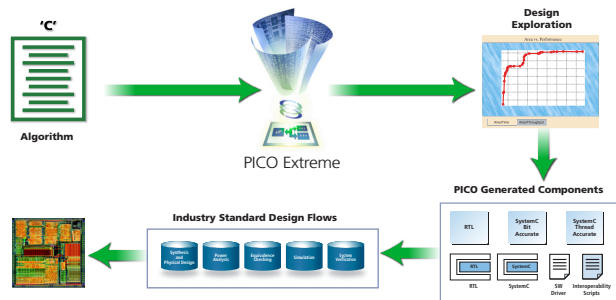
PICO Extreme enables a **recursive system composition methodology**. The designer can define a C procedure as a building block that the compiler schedules and builds as a primitive compute element. A building block can comprise building blocks to an arbitrary depth. This approach is enabled by Synfora's innovative **Tightly Coupled Accelerator Block (TCAB)** technology.

Recursive system composition enhances the ability of the compiler to find better optimization, improving performance and reducing area. In addition, the pre-created blocks ensure that the runtime is reduced.



Overview

Design teams are under growing pressure to create faster, cheaper products. Complex algorithms on silicon differentiate the SoC, but implementing them is expensive and time-consuming. Synfora's PICO Express provides proven, effective and low-risk algorithmic synthesis technology. Now **PICO Extreme** moves you to the next level with algorithmic synthesis for larger, more complex sub-systems.



PICO Algorithmic Synthesis creates efficient hardware from an untimed C algorithm for large, complex subsystems

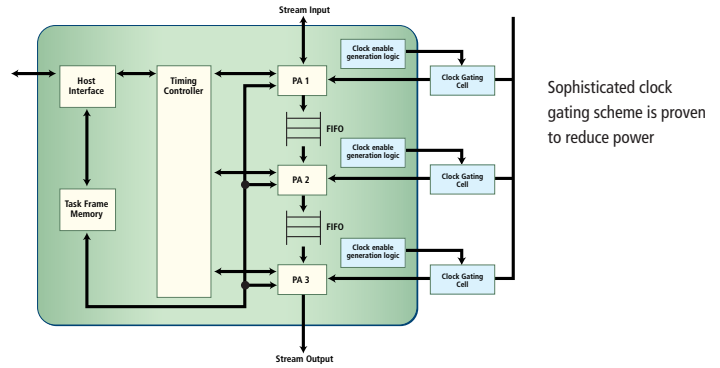
PICO Extreme algorithmic synthesis enables the implementation of dramatically larger and more complex sub-systems and achieves unprecedented results including **reduced power**.

Area can be reduced by 10% or more and runtimes reduced 5x or more, depending on the application.

Advance: Sophisticated clock gating scheme: a designer can gate the clock of a complete processing array (loop nest) as a single entity. PICO Extreme presents a single clock input that can be gated along with the arbitration to signal when the PA can be shut off. This simplifies the scheme, reduces the number of clock gating cells required and improves power efficiency.

Advance: Extraction and export of C-RTL mapping information: third party tools can extract information needed to prove equivalence between C and RTL.

OCP-IP compliant host interface: software drivers and interface to the host enable the sub-system to be controlled from a master processor using memory-mapped IO. PICO Extreme allows the user to select either an OCP-IP or PICO native host interface.



PICO Extreme Key Features

- TCAB technology enables recursive system composition
- Advanced clock gating scheme
- Extracts and exports mapping information for equivalence checking
- Creates OCP-IP compliant interfaces
- Full training and domain-knowledgeable support given

PICO Extreme Key Benefits

- Significantly reduced runtime for larger designs
- Reduced area and power consumption
- Improved hierarchical verification and validation
- Familiar hardware design style

What can I expect to gain from using PICO Extreme?

PICO Extreme reduces time to market by eliminating months of manual RTL design and by providing a comprehensive and robust verification and validation environment which includes automatic RTL testbench creation.

PICO Extreme supports SoC and FPGA prototyping flows and enables designers to build a library of re-usable algorithmic IP for rapid use on a wide range of silicon technologies.

Synfora – premier provider of algorithmic synthesis for SOC and FPGA

The company has a three-pronged focus:

1. Strengthen its lead on algorithmic synthesis technology.

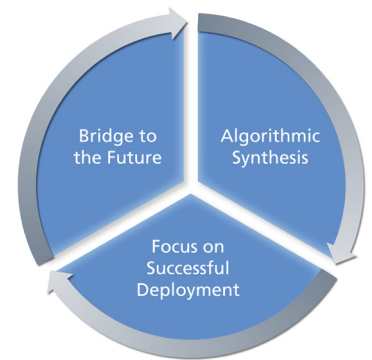
PICO Extreme demonstrates key advances, reflecting the company's determination to enable efficient results from complex algorithms through technology innovation and leadership.

2. Focus on customer deployment.

Synfora dedicates domain-knowledgeable engineers to teach and assist in deploying algorithmic synthesis on challenging projects that demonstrate the benefits of moving to a higher level. This focus provides the best way of transferring practical knowledge to the user.

3. Building bridges to the future.

Synfora is collaborating with industry leaders such as Coware, Synopsys, Cadence, Sequence and others to provide an integrated flow. The successful deployment of an ESL methodology depends on linking algorithmic synthesis to other ESL modeling and analysis tools. Synfora has already built reference flows with key suppliers and will continue to spearhead this effort.



Synfora has a three pronged strategy: Continued leadership of algorithmic synthesis technology; Focus on successful customer deployment; Building bridges to the future with innovation and flows with partners