



Synfora Rolls Out New ASPEN Processor Architecture Designed to Enable and Drive Application Engine Synthesis

At the June Design Automation Conference, Synfora To Demonstrate World's First Application Engine Automatically Configured, Assembled, and Integrated From A Sequential C Source

Mountain View, Calif. — April 26, 2005 — Synfora™, Inc. introduced its new ASPEN™ Architecture, a highly tuned, configurable embedded processor. ASPEN will be a major component of Synfora's second application engine synthesis (AES) product planned for release later this year. Application engine synthesis is ideal for the complex algorithms typically found in consumer applications and promises to reduce system-on-chip (SoC) development time and cost by fifty percent or more.

The ASPEN processor will be automatically integrated with networks of hardware accelerators to provide high-performance, low-cost application engines. The ASPEN processor will drive and control these networks of hardware accelerators. The SoC design process will be supported by a verification environment for testing and validating the application engine in the context of an entire system. Not only will this enable designers to increase productivity, it will also enable more effective silicon.

Synfora CEO Simon Napper said, "The ASPEN architecture represents a major milestone in Synfora's development of application engine synthesis for SoC and system-level design. We are now focused on delivering complex application engines, such as H.264 encoder, in a fraction of the time and resources used in manual design. When DAC attendees see ASPEN integrated with the Synfora PICO Express accelerators, it will be quite an eye opener to them!"

ASPEN Architecture to be demonstrated at the Design Automation Conference (DAC)

At the 42nd DAC in Anaheim, Calif., (www.dac.com) on June 13-17, 2005, Synfora will demonstrate the power of the ASPEN architecture integrated with PICO Express accelerators using an H.264 video encoder. This will be the world's first showing of an application engine being automatically configured, designed, and integrated from a sequential C source.

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About the Synfora ASPEN Architecture

ASPEN represents the next generation of highly scalable, configurable processor architecture optimized for use in complex application engines. The ASPEN architecture can be customized to the application in terms of functionality, for example, instruction set and performance, ranging from low cost to very high performance. For example, it can be configured as a simple controller for multiple hardware accelerators, or as a high performance data processor.

The ASPEN architecture has been designed to integrate tightly with a Synfora PICO Express-generated network of hardware accelerators to provide a complete solution for designing application engines meeting the price, performance, power requirements for consumer SoCs. ASPEN supports features such as programmable interrupts, direct connection to internal registers, and streaming data, all to enable the design of high performance application engines using both processors and networks of hardware accelerators.

ASPEN is a highly parallel architecture based on the state-of-the-art VLIW/EPIC architectures, with high performance features such as multiple instructions issued in a single cycle; multiple clusters to achieve high performance at acceptable cost; predicated or conditional execution to reduce the adverse effect of branches; and rotating registers and special instructions for software pipelining of loops to attain high performance on performance-critical code. ASPEN also includes special features such as saturating and multi-precision arithmetic to address the needs of embedded computing,

"ASPEN brings to life the years of research and development in advanced processor architectures and compiler technology that we conducted at HP Labs and Synfora," said Vinod Kathail, Synfora CTO. "It is very satisfying to see this work result in a product that provides a compelling solution for SoC designers."

About Synfora, Inc.

Founded in 2003, Synfora, Inc. of Mountain View, Calif. is the leading provider of application engine synthesis (AES) software used to design complex systems-on-chips (SoCs). Synfora's patented technology helps to reduce fixed design costs and dramatically speed chip

development and time-to-market. Synfora targets companies in the audio, video, imaging, wireless, and security segments of the IC design market. The company's investors are ATA Ventures, Foundation Capital, and U.S. Venture Partners. For the latest news and information on Synfora, visit www.synfora.com.

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